

What is claimed is:

1. A data output driver of a combination type of a synchronous dynamic random access memory (SDRAM) device  
5 operated in both of a single data rate (SDR) mode and a double data rate (DDR) mode, the data output driver comprising:

a first input/output line connected between a drain of a pull-up transistor and a data input/output pad;

10 a second input/output line connected between a drain of a pull-down transistor and the data input/output pad;

at least one switching unit formed on each of the first input/output line and the second input/output line;  
and

15 at least one resistor parallel-connected with the switch and formed on each of the first input/output line and the second input/output line, wherein the switching unit is turned on or turned off by selecting one of a SDR mode and a DDR mode.

20

2. The data output driver as recited in claim 1, wherein the first and second input/output lines are a first conductive layer and the resistor includes a second conductive layer contacted with the first conductive layer.

3. The data output driver as recited in claim 2,  
wherein the switching unit is turned off between a first  
node and a second node formed on the first conductive layer  
regardless of the second conductive layer, wherein the  
5 first conductive layer is contact with the second  
conductive layer at the first node and the second node.

4. The data output driver as recited in claim 3,  
wherein, in the selected DDR mode, the drain of the pull-  
10 down transistor is connected with the data strobe  
input/output pad through the resistor by turning off the  
switching unit formed on the second output line.

5. The data output driver as recited in claim 2,  
15 wherein a resistance value of the resistor is determined by  
the number of contact nodes formed between the first  
conductive layer and the second conductive layer.

6. The data output driver as recited in claim 2,  
20 wherein the resistance value of the resistor is determined  
by a ratio of width to length of the second conductive  
layer.

7. A data strobe output driver of a combination type

of a synchronous dynamic random access (SDRAM) device operated in both of a single data rate (SDR) mode and a double data rate (DDR) mode, the data strobe output driver comprising:

5           a first input/output line connected between a drain of a pull-up transistor and a data strobe input/output pad;

              a second input/output line connected between a drain of a pull-down transistor and the data strobe input/output pad;

10          a first switch formed on each of the first input/output line and the second input/output line;

              a resistor parallel-connected with the first switch and formed on each of the first input/output line and the second input/output line;

15          a second switch formed on the first input/output line and the second input/output line between the data strobe output pad and an output terminal of the first switch; and

              a third switch formed between an output of the second switch and a ground voltage, wherein the first to the third switches are turned on or turned off by selecting one of

20          the SDR mode and the DDR mode.

8. The data strobe output driver as recited in claim 7, wherein the first and second input/output lines are a

first conductive layer and the resistor includes a second conductive layer contacted with the first conductive layer.

9. The data strobe output driver as recited in claim 5 8, wherein the first switch is turned off between a first node and a second node formed on the first conductive layer regardless of the second conductive layer, wherein the first conductive layer is contact with the second conductive layer at the first node and the second node.

10

10. The data strobe output driver as recited in claim 9, wherein, in the selected DDR mode, the drain of the pull-down transistor is connected with the data strobe input/output pad through the resistor by turning off the 15 first switch formed on the second output line.

11. The data strobe output driver as recited in claim 7, wherein, in the SDR mode, the second switch is turned off and the third switch is turned on, so that a 20 floating state of the first and second input/output lines at the output of the second switch is blocked.

12. The data strobe output driver as recited in claim 8, wherein the second switch and the third switch are

turned off by not forming the first conductive layer locally.

13. The data strobe output driver as recited in  
5 claim 8, wherein a resistance value of the resistor is  
decided by the number of the contact nodes formed between  
the first conductive layer and the second conductive layer.

14. The data strobe output driver as recited in  
10 claim 8, wherein the resistance value of the resistor is  
decided by a ratio of width to length of the second  
conductive layer.

15. A synchronous dynamic random access memory  
15 (SDRAM) of a combination type applying a single data rate  
(SDR) mode and a double data rate (DDR) mode having a data  
output driver, a data strobe output driver and a data mask  
driver, each the data output driver, the data strobe output  
driver and the data mask driver comprising:

20 a first input/output line connected with a drain of a  
pull-up transistor and an input/output pad;

a second input/output line connected with a drain of  
a pull-down transistor and the input/output pad;

a first switching unit connected with each of the

first input/output line and the second input/output line at the drains of the pull-up transistor and the pull-down transistor;

5 a first resistor parallel-connected with the first switch formed on each of the first input/output line and the second input/output line;

a second switch formed on each of the first input/output line and the second input/output line adjacent to the input/output pad;

10 a second resistor parallel-connected with the second switch and formed on each of the first input/output line and the second input/output line; and

15 a third switch formed on each of the first input/output line and the second input/output line allocated between the first switch and the second switch, wherein the first to the third switches are turned on or off by selecting one of the SDR mode and the DDR mode.

16. The SDRAM as recited in claim 15, wherein the 20 data strobe output driver further comprises a fourth switch formed between the first and the second input/output lines and a ground voltage.

17. The SDRAM as recited in claim 16, wherein each

of the first input/output line and the second input/output line is a first conductive layer, and the first resistor and the second resistor are a second conductive layer contacted with the first conductive layer.

5

18. The SDRAM as recited in claim 17, wherein the first and second switches are turned off between a first node and a second node formed on the first conductive layer regardless of the second conductive layer, wherein the 10 first conductive layer is contact with the second conductive layer at the first node and the second node.

19. The SDRAM as recited in claim 18, wherein, in the selected DDR mode, the drain of the pull-down 15 transistor is connected with the data strobe input/output pad through the first and second resistors by turning off the switching unit formed on the second output line.

20. The SDRAM as recited in claim 16, wherein a 20 floating state of the first input/output line and the second input/output line adjacent to an output terminal of the second switch is blocked by turning off the third switch in the SDR mode and turning on the fourth switch in the DDR mode.

21. The SDRAM as recited in claim 16, wherein each of the first input/output line and the second input/output line is formed with the first conductive layer, and the second to the fourth switches are turned off by not forming 5 the first conductive layer locally.

22. The SDRAM as recited in claim 17, wherein a resistance value of the resistor is decided by the number of the contact nodes formed between the first conductive 10 layer and the second conductive layer.

23. The SDRAM as recited in claim 17, wherein the resistance value of the resistor is decided by a ratio of width to length of the second conductive layer.